SOFT MUTE CIRCUIT

Cross-reference to related application

sub a1

This application includes disclosure contained in Application No. 09/____________, filed December 30, 1999, entitled *"Band-by-Band Full Duplex Communication"*, assigned to the assignee of this invention, and now U.S. Patent ________________. The entire contents of the earlier application is incorporated herein by reference.

BACKGROUND OF THE INVENTION

This invention relates to a soft mute circuit; that is, a circuit for masking transients in an audio electronic device. As used herein, a "transient" is an abrupt change in the operation of a circuit or a spurious signal caused by such abrupt change.

Anyone who has ever put on earphones before plugging the earphones into an operating radio, stereo, or cellular telephone knows well the sound of transients. Other transients occur during the operation of audio electronic devices. In a device such as a telephone or a hearing aid, the transients can be particularly annoying. Such transients arise from switching circuitry within the device as the device changes state. Telephone systems, for example, have at least two channels and a plurality of filters in each channel. The various combinations of channels and filters are switch selected and the changes can be heard easily, to the annoyance of the user.

In the prior art, such transients were generally handled by filtering or by carefully matching voltage levels. U.S. Patent 4,983,927 (Torazzina) discloses a bias circuit that causes a power amplifier to go through "mute" and "standby" states when the amplifier changes 330/51 267

from normal operation to "cut-off" for blocking transients.

Unlike the Torazzina patent, it is desired to selectively mute signals from a plurality of sources. It is also desired to control the depth and duration of the mute better.

In view of the foregoing, it is therefore an object of the invention to provide an improved mute circuit for unobtrusively masking transients in an audio device.

Another object of the invention is to provide a mute circuit that can operate on several signals in any combination.

A further object of the invention is to provide a mute circuit wherein the depth and duration of the mute are adjustable.

Another object of the invention is to provide a soft mute for a telephone.

SUMMARY OF THE INVENTION

The foregoing objects are achieved in this invention in which the soft mute circuit includes a programmable amplifier controlled by a register. Data is stored in the register from an adder that combines the current data in the register with a second number for increasing or decreasing the gain of the amplifier. A summation circuit includes a plurality of inputs coupled by gates to a summation node and the summation node is coupled to an input of the programmable amplifier. The gates are controlled by suitable logic for selecting input signals in any combination. A control loop maintains the gain of the amplifier at a predetermined level.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the invention can be obtained by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a soft mute circuit constructed in accordance with a preferred embodiment of the invention;

FIG. 2 is a chart illustrating the operation of the circuit of FIG. 1;

FIG. 3 is a more detailed diagram of the variable gain circuit represented by block 12 in FIG. 1;

FIG. 4 is a schematic of summation circuit 11 in FIG. 1; and

FIG. 5 is a block diagram of a telephone incorporating a mute circuit constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

In FIG. 1, soft mute circuit 10 includes summation circuit 11 and variable gain circuit 12. Inputs 13, 14, 15, 16, and 17 are from separate signal sources [not shown] and are selected in accordance with data on input 22 by way of decoder 21. In the figures, plural lines are represented by a single heavy line rather than a plurality of thinner lines. Input 22 is actually five inputs, one enable line for each signal line.

A multiplex circuit could be used instead of summation circuit 11. An advantage of having a summation circuit shown is that the signal lines can be summed in any combination on output line 23. Circuit 12 includes a variable gain amplifier that adjusts the amplitude of the signal on line 23 and couples the adjusted signal to

circuit output 27. Output 28 provides the summed signals unadjusted.

Circuit 12 is controlled by enable input 24 and gain input 25. In a preferred embodiment of the invention, gain input 25 is actually an eight bit data bus. The data on the bus determines the maximum amplitude of the signal on output 27. The operation of soft mute circuit 10 is illustrated in FIG. 3. Assuming unity (zero dB) gain as an initial condition, a logic "1" on enable input 24 causes the gain of circuit 12 to decrease incrementally for as long as pin 24 remains at a logic "1" or until a minimum gain is reached.

The gain remains at minimum 31 (FIG. 2), represented by gap 32, for as long as a logic "1" is applied to input 24. When a logic "0" is applied to input 34, the gain of the circuit increases to a value corresponding the data on input 25. The gain can be more or less than zero dB and can remain at some intermediate value, represented by line 34, for some time before being changed to another value in accordance with the data on input 25.

FIG. 3 illustrates circuit 12 in greater detail. Programmable gain amplifier 41 has a signal input coupled to line 23 and a control input coupled to register 42. The output of register 42 is also coupled to one input of adder 43. Comparator 44 compares the output from adder 43 with the data on gain input 25 and, if the output is equal to or greater than the data, the data is locked in register 42 and the gain of amplifier remains constant until the next enable signal on input 24.

Enable input 24 is coupled to the add/subtract input of adder 43, causing the data on bus 46 to be added to, or subtracted from, the data on bus 47. In this way, the rate of change, i.e. the size of the steps shown in FIG. 2, can be adjusted to suit a particular application. The size of the step need not be the same for counting up as for counting down. In one embodiment of the invention,

having a clock of 44.1 kHz., amplifier 41 had a maximum gain of approximately 1.93 and unity gain at $B4_{16}$ (10110100). Counting from 0 to FF_{16} took 5.8 milliseconds, incrementing every twenty-three microseconds (one count per clock cycle). This rate does not cause a noticeable sound and is not perceptible as fading.

Changing the data on input 46 changes the slope of the stairstep shown in FIG. 2. For example, if the count in register 42 is incremented by two on each clock cycle, the gain decreases, or increases, twice as fast. The duration of the gap 32 depends upon the application and could be several hours or more or could be as short as one clock cycle. Enable 24 (FIG. 3) does not have to remain a logic "1" until a minimum gain is reached, although for most applications this would be the case. The actual value of minimum gain depends upon the particular amplifier but should be at least -40 dB.

FIG. 4 illustrates summation circuit 11 in greater detail. In one embodiment of the invention, switched capacitor circuits and differential signals were used for improved noise immunity. FIG. 4 illustrates one half of the circuit for simplicity. The positive and negative halves of the circuits are the same. The circuit was clocked at 44.1 kHz., as noted above.

Summation circuit 11 includes a plurality of identical sections having their outputs coupled to a common node. Each section includes a first input, such as input 13, for receiving a signal, and a gate, such as gate 51, for blocking or passing a signal to storage capacitor 52. One side of storage capacitor 52 is coupled to gate 51 and the other side of the storage capacitor is coupled to node 53.

Gate 51 is controlled by NAND gate 55 having a first input coupled to clock enable 56 in common with the other NAND gates. A second input to NAND gate 55 is coupled to

section enable input 57. Thus, the sections are controllable individually and as a group. The output of NAND gate 55 is coupled through an inverter to the control electrode of gate 51. The inverter provides the correct logic level for gate 51.

Depending upon the data on the individual enable inputs, one, some, or all of the signals on inputs 13-17 are coupled to node 53. The discharge currents of the capacitors are summed and applied to variable gain section 12 (FIG. 3). Although implemented in a preferred embodiment as a switched capacitor circuit, other topologies can be used instead, either analog or digital.

FIG. 5 shows the invention used in the noise reduction circuitry of a telephone. Noise in a telephone, including cellular telephones, is any unwanted sound and includes echoes of the voices of the parties to a call. Many techniques have been developed to improve the clarity of the sound in a telephone. One such technique uses what is known as a comb filter; i.e. a plurality of parallel filters wherein band pass filters alternate with band stop filters. As described in the above-identified copending application, each bank of filters in FIG. 5 can be configured by controller 60 to mimic a comb filter, by selecting alternate filters, or to provide a variety of other combinations.

Soft mute circuits 62 and 63, constructed as shown in FIG. 1, provide a multiplexing and summation function in addition to a soft mute function. For example, controller 61 can couple the outputs of the even numbered filters in bank "A" to line output 65 using soft mute circuit 62 and couple the outputs of the odd numbered filters in bank "B" to speaker 66 using soft mute circuit 63. Any change in configuration is not detected by a user because the signals are attenuated during the change but are attenuated only briefly. On the other hand, the

attenuation may continue for some time, e.g. when providing half duplex operation.

The invention thus provides a versatile mute circuit having plural functions for unobtrusively masking transients in an audio device. The mute circuit can operate on several signals in any combination and the depth and duration of the mute are independently adjustable.

Having thus described the invention, it will be apparent to those of skill in the art that various modifications can be made within the scope of the invention. For example, instead of using enable 24 for controlling the duration of the mute, one could add a programmable timer triggered by a signal on input 24. The control loop in FIG. 3 could operate on adder 43 instead of register 42 for freezing data when a particular gain were reached, e.g. by coupling zeros to input 46. Programmable gain amplifier can be configured to have gain inversely proportional, rather than proportional, to the data from register 42.